IN THE SPECIFICATION

Please amend paragraph [0015] as follows:

[0015] **Figure 2** illustrates commit CPU 110. In one embodiment of the invention, commit CPU 110 comprises decoder 211, scoreboard 214, register file 212, and execution units 213. Likewise, **Figure 3** illustrates speculative CPU 120. In one embodiment of the invention, speculative CPU 120 comprises decoder 321, scoreboard 324, register file 322, and execution units 323. L2 cache 170 and L1 cache 175 are shared by commit CPU 110 and speculative CPU 120. In one embodiment of the invention, multiprocessor 100 is capable of executing explicitly multithreaded programs. In another embodiment, multiprocessor 100 is capable of executing single-threaded applications while using a multi-thread environment without converting the single-threaded application to an explicit multiple-thread application.